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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,046	08/28/2003	Toru Takayama	0756-7193	7230

31780 7590 07/20/2007

ERIC ROBINSON
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER	
NGUYEN, THANH T	

ART UNIT	PAPER NUMBER
2813	

MAIL DATE	DELIVERY MODE
07/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/650,046	TAKAYAMA ET AL.	
	Examiner	Art Unit	
	Thanh T. Nguyen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-5,8,13,18,23,28,33,36-43,45,47-57 and 74-81* is/are pending in the application.

4a) Of the above claim(s) *none* is/are withdrawn from consideration.

5)☒ Claim(s) *36-43,45 and 47-57* is/are allowed.

6)☒ Claim(s) *3,5,8,13,18,23,28,33 and 74-80* is/are rejected.

7)☐ Claim(s) *4 and 81* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 4/27/07 have been fully considered but they are not persuasive.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 5, 8, 13, 28, 33, 74, 76-77, 79-80 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joo et al. (U.S. Patent Publication No. 2002/0056839) in view of Yamazaki et al. (U.S. Patent Publication No. 2001/0049163A1).

Referring to figures 1-9f, Joo et al. teaches a manufacturing method for a semiconductor device comprising:

Forming at least first and second semiconductor layers (33, amorphous silicon) that are divided from each other in an island-like shape over a substrate surface having an insulating surface (32, silicon oxide, see figures 3a), wherein each of the first and second semiconductor layers includes a region to become at least a channel region of a thin film transistor (see paragraph# 26, figure 3a);

Forming a conductive layer (35, doped polysilicon) covering an entire surface of each of the first and second semiconductor layers (33) with an insulating layer (34) interposed the between (see figure 3b, paragraph# 28); and

Selectively heating the first and second semiconductor layer by irradiating an incoherent electromagnetic wave within a wavelength band ranging at least from a visible light band to an infrared band to thereby conducting heat treatment on the first and second semiconductor layers and the insulating layer, wherein the conductive layer extends beyond each periphery of the first and second semiconductor layers at least when the selected heating of the first and second semiconductor layers is performed (see paragraphs# 32, figure 3f). It is inherent that heating the conductive layer, the semiconductor layers and the insulating layer will also heated.

Regarding to claims 8, 76, substrate is a glass substrate (see paragraph# 23).

Regarding to claims 13, 77, the substrate is quartz or sapphire (see paragraph# 23).

Regarding to claims 28, 79, forming a second conductive layer (36, nickel, see paragraph# 29) on the conductive layer (35) and forming a part of a gate electrode (35) using the conductive layer (35, see figures 3c-3d(1)).

Regarding to claim 74, a manufacturing method for a semiconductor device comprising:

Forming a semiconductor layer (33, amorphous silicon) over a substrate (30);

Forming an insulating layer (34, silicon oxide) over the semiconductor layer (33);

Forming a conductive layer (35) over the semiconductor layer with the insulating layer (34) interposed there between;

Selectively heating the semiconductor layer by using a heat source capable of radiating an incoherent electromagnetic wave within a wavelength band ranging at least a visible light

band to an infrared band (see paragraphs# 32, figure 3f). It is inherent that heating the conductive layer, the semiconductor layers and the insulating layer will also heated.

However, the reference does not teach the conductive films extends beyond each periphery of the first and second semiconductive layer when the heating of the first and second semiconductive layers is performed, the time range, and temperature range.

Yamazaki et al. teaches the conductive films extends beyond each periphery of the first and second semiconductive layer when the heating of the first and second semiconductive layers is performed (see paragraphs# 254, 294, meeting claims 3, 74. It is inherent that heating the conductive layer, the semiconductive layer and the insulating layer will also heated), the incoherent electromagnetic wave is irradiated for 30-300 seconds (see paragraph# 254, meeting claim 5), the heat treatment is performed at a temperature not less than a distortion point of the substrate (see paragraph# 254, 294, heating at the temperature 700-1000°C which is greater than 700°C (at the distortion point), meeting claims 33, 80).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form plurality of semiconductive island, etching the conductive layer after the selective heating for 30-300 second at the temperature greater than distortion point of the substrate in process of Joo et al. as taught by Yamazaki et al. because forming plurality of semiconductor island would provide plurality of thin film transistors, etching the conductive layer to form the gate electrode, heating to crystallized the layer as well as to activate the impurity added to the film.

Claims 18, 23, 75, 78 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joo et al. (U.S. Patent Publication No. 2002/0056839) in view of Yamazaki et al. (U.S. Patent

Publication No. 2001/0049163A1) as applied to claims 3, 5, 8, 13, 28, 33, 74, 76-77, 79-80 above in view of Yamazaki et al. (U.S. Patent Publication No. 2002/0000551).

Joo et al. in view of Yamazaki et al. teaches a method of forming a semiconductor device. However, Yamazaki does not teach the substrate has a transmittance of 50 % or higher with respect to the electromagnetic wave within the wavelength band, forming a first conducting film comprising metal nitride and forming a second conducting film over the first conducting film as a part of the gate electrode.

Regarding to claims 23, 78, the conductive film comprises metal nitride (see paragraph# 245).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to form a quartz substrate in process of Joo et al. as taught by Yamazaki et al. in order for light transparent or to form an insulating substrate, forming the conductive film on the gate insulating film in order to form gate electrode for TFT device.

Regarding to claims 18, 75, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to optimize the a transmittance of 50 % or higher with respect to the electromagnetic wave within the wavelength band, since it has been held that where the general conditions of a claim are disclosed in the prior art (i.e.- a transmittance of 50 % or higher with respect to the electromagnetic wave within the wavelength band), discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 (CCPA 1955).

The specification contains no disclosure of either the critical nature of the claimed arrangement (i.e.- a transmittance of 50 % or higher with respect to the electromagnetic wave

within the wavelength band) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the applicant must show that the chosen limitations are critical. In re Woodruff, 919 F.2d 1575, 1578 (FED. Cir. 1990).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to form the substrate has a transmittance of 50 % or higher with respect to the electromagnetic wave within the wavelength band in process of Joo et al. in order to optimize the process.

Allowable Subject Matter

Claims 4, 81 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

None of the prior art alone or in combination teaches the step of etching the conductive layer after the selective heating of the semiconductor layer to form a gate electrode over the semiconductor layer.

Claims 36-43, 45, 47-57 are allowed. Because none of the prior art alone or in combination teaches a heating the substrate by radiation heating from a first heat source and form the layers on the substrate, then heating the layer by using a second heat source for radiating the incoherent electromagnetic wave.

Response to Arguments

Applicant's arguments filed 4/27/07 have been fully considered but they are not persuasive.

Applicant contends that Joo does not teach the conductive layer extend beyond the periphery of the semiconductive layer. In response to applicant that Yamazaki et al. teaches the conductive films extends beyond each periphery of the first and second semiconductive layer when the heating of the first and second semiconductive layers is performed (see paragraphs# 254, 294. It is inherent that heating the conductive layer, the semiconductive layer and the insulating layer will also heated).

Examiner agreed that neither Yamazaki nor Joo teaches the step of etching the conductive layer after the selective heating of the semiconductor layer to form a gate electrode over the semiconductor layer.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (571) 272-1702. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pairdirect.uspto.gov. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

Thanh Nguyen
Patent Examiner
Patent Examining Group 2800

TTN